UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 7,468,536 B2
APPLICATION NO. : 11/707403
DATED : December 23, 2008
INVENTOR(S) : Vijay Parthasarathy

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 4, Lines 52-58 reads:

"In one embodiment, for a 2mm × 2mm die with 60μm high pillars, adequate stress relief is provided in a HVFET with an on-resistance of about 1 ohm utilizing a layout comprising four racetrack transistor sections separated by dummy silicon pillars, each having a pitch (y-direction) of about 13μm and a length (x-direction) of about 450μm."

It should read:

"In one embodiment, for a 2mm × 2mm die with 60μm high pillars, adequate stress relief is provided in a HVFET with an on-resistance of about 1 ohm utilizing a layout comprising four racetrack transistor sections separated by dummy silicon pillars, each having a pitch (x-direction) of about 13μm and a length (y-direction) of about 450μm."

Signed and Sealed this
Fourth Day of September, 2012

David J. Kappos

David J. Kappos
Director of the United States Patent and Trademark Office